The Office Action notes that the application is a continuation-in-part of Application No. 08/879,696 which has issued as U.S. Patent No. 6,094,527 to Tsukamoto et al. The Office Action states that there does not appear to be new matter in the subject application as compared with the disclosure in U.S. Patent No. 6,094,527. The Office Action further states that the addition of reader/writer 16 and removable storage media 16a in Fig. 2 do not constitute the addition of new matter because hard disk 13 contains computer readable media with read/write ability.

In view of the remarks in the Office Action, it is Applicants' understanding that the Examiner deems the claims of the subject application to be fully supported by, and therefore is entitled to the benefit of priority of, parent application no. 08/879,696.

Applicants respectfully direct the Examiner's attention to, for example, the specification at page 6, line 7 through page 7, line 7 which further describe elements 16a and 16.

Claims 25, 29, and 37 were rejected under the judicially created doctrine of obviousness-type double patenting as allegedly unpatentable over claim 4 of U.S. Patent No. 6,094,527. Claims 33 and 39 were rejected under the judicially created doctrine of obviousness-type double patenting as purportedly unpatentable over claim 6 of U.S. Patent No. 6,094,527. Claim 1 was rejected under the judicially created doctrine of obviousness-type double patenting over claim 1 of U.S. Patent No. 6,094,527. Claim 17 was rejected under the judicially created doctrine of obviousness-type double patenting as allegedly unpatentable over claim 3 of U.S. Patent No. 6,094,527.

Applicants maintain that the claims of the subject application are patentably distinct

from the claims of U.S. Patent No. 6,094,527 for at least the following reasons.

For example, claim 4 of U.S. Patent No. 6,094,527 recites an apparatus for estimating power consumption of an integrated circuit. Each of claims 25 and 29 of the subject application claims a programmable computer for estimating power consumption of an integrated circuit, and claim 37 claims a programmed computer for estimating power consumption of an integrated circuit. Even if claims 25, 29, and 37 of the subject application can hypothetically be analogized to claim 4 of U.S. Patent No. 6,094,527, the comparison merely shows that claims 25, 29, and 37 of the subject application are species of a class of apparatuses for estimating power consumption of an integrated circuit. Applicants respectfully submit that species claims cannot be rendered unpatentable, even under the judicially created doctrine of obviousness-type double patenting, by patent claims to the broader class.

These same reasons apply similarly to the comparisons of claims 33 and 39 of the subject application and claim 6 of U.S. Patent No. 6,094,527.

In addition, each of claims 1 and 17 claims a computer readable medium including computer executable code stored thereon for estimating power consumption of an integrated circuit. The claimed invention can be regarded as species of a class of apparatuses for estimating power consumption of an integrated circuit. Each of claims 1 and 3 of U.S. Patent No. 6,094,527, in contrast, each recites a method for estimating power consumption of an integrated circuit. Applicants respectfully submit that method claims 1 and 3 of U.S. Patent No. 6,094,527 cannot render unpatentable claims 1 and 17 of the subject application, even under the judicially created doctrine of obviousness-type double patenting.

Accordingly, Applicants submit that independent claims 1, 17, 25, 29, 33, 37, and 39

are patentable over U.S. Patent No. 6,094,527.

Independent claim 29 was objected to under 37 C.F.R. §1.75 as allegedly being a substantial duplicate of independent claim 25.

Applicants respectfully point out that MPEP §706.03(k) states that "court decisions have confirmed applicant's right to restate (i.e., by plural claiming) the invention in a reasonable number of ways. Indeed, a mere difference in scope between claims has been held to be enough."

A comparison of claims 29 and 25 shows that claim 29 recites features not recited in claim 25. One non-limiting example of a feature recited in claim 29 that is not recited in claim 25 is that an estimate for a first value of electric power consumed by the basic cells is based on pre-established power consumption data for each logic state at each input and output terminal of the basic cells, among other factors.

In addition, Applicants respectfully submit that such an objection is premature, since neither claim 25 or 29 have been allowed.

Accordingly, Applicants respectfully request the objection under 37 C.F.R. §1.75 be withdrawn.

The Office Action states that the broadest possible interpretation has been given to the claims, and interprets the "logic of basic and mega cells of an integrated circuit" as logic gates in an Application Specific Integrated Circuit (ASIC), and in the case of claims 9 and 38 a Field Programmable Gate Array (FPGA). According to the Office Action, mega cells have been construed in the Office Action to mean the groups of transistors at the gate level of ASICs or FPGAs.

Applicants respectfully disagree. The subject application explicitly incorporates by reference the entire contents of parent application no. 08/879,696 (see the present application, page 1 under "Cross-Reference to Related Applications"). Parent application no. 08/879,696 (at page 2, lines 17-18) states that basic cells are relatively simple logic gates including, for example, AND, OR, NOR, and NOT logic gates. According to parent application no. 08/879,696 (at page 2, lines 18-22), a mega cell may be defined by functional circuit blocks, functions of which are described by the hardware description language during logic simulations, and those cells whose construction is not explicitly represented by basic cells. Examples of mega cells include CPUs, DSPs, ROMs, and ROMs.

Claims 1-39 were rejected under 35 U.S.C. §103(a) as allegedly unpatentable over U.S. Patent 5,943,487 to Messerman et al. in view of U.S. Patent No. 6,324,678 to Dangelo et al., and further in view of U.S. Patent No. 5,867,397 to Koza et al., and the Microsoft Press Computer Dictionary, Third Edition. Applicants have carefully considered the Examiner's comments and the cited art, and respectfully submit that independent claims 1, 9, 17, 25, 29, 33, and 37-39 are patentable over the cited art, for at least the following reasons.

Independent claim 1 relates to a computer readable medium including computer executable code stored thereon, for estimating power consumption of an integrated circuit. The computer executable code includes (a) code for simulating logic of basic and mega cells of the integrated circuit, (b) code for estimating a current consumed by the mega cells by obtaining logic states for each mega cell, determining an average operation frequency for each logic state, and determining an alternating current component and a direct current component for each logic state to calculate the current consumed by the mega cells for estimating a first

value of electric power consumed by the mega cells based on the logic simulations and pre-established power consumption data, (c) code for estimating a current consumed by the basic cells for estimating a second value of electric power consumed by the basic cells based on the logic simulations and pre-established power consumption data, and (d) code for combining the first and second values to obtain the power consumption of the integrated circuit.

Messerman et al., as understood by Applicants, relates to a method for reducing a full resistor network extracted from an integrated circuit polygon layout, and then simulating operation of the reduced resistor network to determine operational voltages at the nodes of the reduced resistor network. The operational voltages at the nodes of the full resistor network can then be determined, as well as the operational current through a resistor utilizing the node voltages in the full resistor network (col. 3, lines 33-43, col. 9, lines 8-16, and col. 10, lines 30-38).

Dangelo et al., as understood by Applicants, relates to a method and system for creating and validating a low-level description of an electronic design. Static power dissipation is calculated by multiplying a leakage current (static current draw) of a representative logic device (gate) and a supply voltage, and summing the total number of logic devices (gates) (col. 36, line 66 to col. 37, line 17). Dynamic power dissipation in a CMOS device is calculated using output load capacitance, supply voltage, clock cycle, and the number of switching transitions per clock cycle as parameters (col. 37, lines 18-55). Power estimation at a system level uses statistical models that take into account critical parameters (col. 39, lines 18-67). Power estimation at algorithmic (functional), behavioral and register transfer levels utilizes more information. Control logic size and associated power dissipation are estimated

from the number of states in the design and the complexity of Boolean equations activating elements of the data path in the circuit (col. 40, line 63 to col. 41, line 24).

However, Applicants find no teaching or suggestion in Dangelo et al. (or in the other cited references) of, for example, code for estimating a current consumed by the mega cells by obtaining logic states for each mega cell, determining an average operation frequency for each logic state, and determining an alternating current component and a direct current component for each logic state to calculate the current consumed by the mega cells for estimating a first value of electric power consumed by the mega cells based on the logic simulations and pre-established power consumption data, as recited in independent claim 1.

Koza et al., as understood by Applicants, relates to a method and apparatus for automated design of complex structures such as circuits using genetic operations. The behavior of the developed structure is determined, compared to the predetermined design goals and then evolved until it meets the design goals (Fig. 1A, and col. 33-64). Simulations and fitness measures as discussed in Koza et al. focus solely on circuit behavior in terms of inputs and outputs (col. 80, line 46 to col. 83, line 35).

Applicants find no teaching or suggestion in the cited art of a computer readable medium including computer executable code stored thereon, the code for estimating power consumption of an integrated circuit, comprising code for simulating logic of basic and mega cells of the integrated circuit, code for estimating a current consumed by the mega cells by obtaining logic states for each mega cell, determining an average operation frequency for each logic state, and determining an alternating current component and a direct current component for each logic state to calculate the current consumed by the mega cells for estimating a first

value of electric power consumed by the mega cells based on the logic simulations and pre-established power consumption data, code for estimating a current consumed by the basic cells for estimating a second value of electric power consumed by the basic cells based on the logic simulations and pre-established power consumption data, and code for combining the first and second values to obtain the power consumption of the integrated circuit, as recited in independent claim 1.

Accordingly, Applicants submit independent claim 1 is patentable over the cited art. Independent claims 9, 17, 25, 29, 33, and 37-39 are believed to be patentable over the cited art for at least similar reasons.

In addition, Applicants find no teaching or suggestion in the cited art of code for compiling a table which tabulates data of electric power consumed by mega cells of the integrated circuit during operation, and code for simulating logic of the mega cells and basic cells of the integrated circuit, wherein data from the table is used when simulating logic of the mega cells, as recited in independent claims 17 and 39. Independent claim 33 is believed to be patentable for at least similar reasons.

The Office is hereby authorized to charge any additional fees that may be required in connection with this response and to credit any overpayment to our Deposit Account No. 03-3125.

If a petition for an extension of time is required to make this response timely, this paper should be considered to be such a petition, and the Commissioner is authorized to charge the requisite fees to our Deposit Account No. 03-3125.

If a telephone interview could advance the prosecution of this application, the Examiner is respectfully requested to call the undersigned attorney.

Entry of this response and allowance of this application are respectfully requested.

Respectfully submitted,

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